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EXAMINER	
LOO, JUVENA W	
ART UNIT	**PAPER NUMBER**
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,392	NAIK ET AL.	
	Examiner	Art Unit	
	Juvena W. Loo	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *December 22, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13,15-21 and 23-30* is/are rejected.

7)☒ Claim(s) *7,14 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is in response to application filed on December 22, 2003 in which claims 1 to 30 are presented for examination.

Status of Claims

Claims 1 - 30 are pending, of which claims 1, 10, 15, 23, and 28 are in independent form.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 6, 8 – 13, 15 – 21, and 23 - 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Rusu et al. (Patent number: 6,137,807).

Regarding claim 1, Rusu discloses a method comprising receiving a plurality of packets from an inflow of a single packet flow (Figure 1A, 60; Figure 4); enqueuing a plurality of packet pointers into multiple link lists, each one of the plurality of packet pointers designating one of the plurality of packets from the single packet flow (Figure 4,

130 and 131; column 1, lines 34 – 38; column 3, lines 61 - 64; column 4, lines 54 - 57: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list); and dequeuing the plurality of packet pointers from the multiple link lists to transmit the plurality of packets along an outflow of the single packet flow (Figure 1A, 61; Figure 4).

Regarding claim 2, Rusu discloses all the limitations of claim 1. Additionally, Rusu discloses that enqueuing the plurality of packet pointers further comprises enqueuing the plurality of packet pointers into the multiple link lists using a round robin enqueuing scheme between the multiple link lists (Figure 4, 130 and 131; Figure 5; column 1, lines 34 – 38; column 3, lines 61 - 64; column 4, lines 54 – 57; column 5, lines 27 – 31: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list. The round-robin weighted process is used to provide for storing incoming data, utilizing the link list with the highest priority).

Regarding claim 3, Rusu discloses all the limitations of claim 2. Additionally, Rusu discloses that dequeuing the plurality of packet pointers further comprises dequeuing the plurality of packet pointers from the multiple link lists in a same order as enqueuing the plurality of packet pointers into the multiple link lists (Figure 6; column 4, lines 54 – 57; column 5, lines 20 – 35: data in the memory banks is maintained in the

form of queues on a first in first out (FIFO) basis, organized by a link list. The output arbitration subsystem uses the same round-robin weighted process as in the input subsystem to buffer and re-segment the data from a chosen queue memory into an acceptable concatenated form for output).

Regarding claim 4, Rusu discloses all the limitations of claim 1. Additionally, Rusu discloses that the multiple link lists comprise two link lists (Figure 4, 130 and 131) and enqueuing the plurality of packet pointers into the multiple link lists further comprises alternating enqueues of each of the plurality of packet pointers between the two link lists (Figure 5; column 5, lines 27 – 31: the round-robin weighted process is used to provide for storing incoming data, utilizing the link list with the highest priority).

Regarding claim 5, Rusu discloses all the limitations of claim 4. Additionally, Rusu discloses that dequeuing the plurality of packet pointers from the two link lists further comprises alternating dequeues of each of the plurality of packet pointers from the two link lists in a same order as the alternating enqueues (Figure 6; column 4, lines 54 – 57; column 5, lines 20 – 35: data in the memory banks is maintained in the form of queues on a first in first out (FIFO) basis, organized by a link list. The output arbitration subsystem uses the same round-robin weighted process as in the input subsystem to buffer and re-segment the data from a chosen queue memory into an acceptable concatenated form for output).

Regarding claim 6, Rusu discloses all the limitations of claim 1. Additionally, Rusu discloses that receiving multiple packet flows, each one of the multiple packet

flows including a plurality of packets (Figure 1, 60 and 70; Figure 4); enqueuing a plurality of packet pointers for each of the multiple packet flows into multiple link lists, each one of the plurality of packet pointers designating one of the plurality of packets of each of the multiple packet flows (Figure 4, 130 and 131; column 1, lines 34 - 38; column 3, lines 61 - 64; column 4, lines 54 - 57: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list); and dequeuing the plurality of packet pointer for each of the multiple packet flows from each of the multiple link lists to transmit each of the plurality of packets along a corresponding outflow of each of the multiple packet flows (Figure 1, 61; Figure 4).

Regarding claim 8, Rusu discloses all the limitations of claim 1. Additionally, Rusu discloses the multiple link lists comprise multiple physical link lists having multiple link list elements, each link list element including one of the plurality of packet pointers and a next element pointer (Figures 4 and 7, 130, 131, 140, and 145: two physical memory or queue banks maintained by the queue controller with the control memory).

Regarding claim 9, Rusu discloses all the limitations of claim 1. Additionally, Rusu discloses that the single packet flow comprises a single data packet flow along a network path (Figure 1A, 60 and 61; column 4, lines 20 – 23: the system can be configured to have a single input bus with a single physical memory bank with two logical queue memory banks).

Regarding claim 10, Rusu discloses a method comprising receiving a plurality of packets from a packet inflow (Figure 1A, 60; Figure 4); enqueuing the plurality of packets from the packet inflow into multiple physical queues (Figure 4, 130 and 131; column 1, lines 34 - 38; column 3, lines 61 - 64; column 4, lines 54 - 57: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list); and dequeuing the plurality of packets from the multiple physical queues to transmit the plurality of packets along a packet outflow (Figure 1A, 61; Figure 4).

Regarding claim 11, Rusu discloses all the limitations of claim 10. Additionally, Rusu discloses enqueuing the plurality of packets into the multiple physical queues comprises enqueuing the plurality of packets into the multiple physical queues using a round robin enqueuing scheme between the multiple physical queues (Figure 4, 130 and 131; Figure 5; column 1, lines 34 – 38; column 3, lines 61 - 64; column 4, lines 54 – 57; column 5, lines 27 – 31: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list. The round-robin weighted process is used to provide for storing incoming data, utilizing the link list with the highest priority).

Regarding claim 12, Rusu discloses all the limitations of claim 11. Additionally, Rusu discloses dequeuing the plurality of packets from the multiple physical queues comprises dequeuing the plurality of packets from the multiple physical queues in a same order as the plurality of packets were enqueued into the multiple physical queues (Figure 6; column 4, lines 54 – 57; column 5, lines 20 – 35: data in the memory banks is maintained in the form of queues on a first in first out (FIFO) basis, organized by a link list. The output arbitration subsystem uses the same round-robin weighted process as in the input subsystem to buffer and re-segment the data from a chosen queue memory into an acceptable concatenated form for output).

Regarding claim 13, Rusu discloses all the limitations of claim 10. Additionally, Rusu discloses a method comprising receiving multiple pluralities of packets from corresponding multiple packet inflows (Figure 1A, 60 and 70; Figure 4); enqueuing each of the multiple pluralities of data packets from the corresponding multiple packet inflows into corresponding multiple physical queues (Figure 4, 130 and 131; column 1, lines 34 - 38; column 3, lines 61 - 64; column 4, lines 54 - 57: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list); and dequeuing each of the multiple pluralities of packets from the corresponding multiple physical queues to transmit each of the multiple pluralities of packets along corresponding packet outflows (Figure 1A, 61 and 71, Figure 4).

Regarding claim 15, Rusu discloses a machine-accessible medium that provides instructions that, if executed by a machine, will cause the machine to perform operations comprising enqueuing a plurality of packet pointers into multiple physical queues, the plurality of packet pointers to each point to a memory location temporarily having stored therein one of a corresponding plurality of packets, the corresponding plurality of packets received from a packet flow via a first network link (Figures 4, 5, and 7, 130, 131, and 145; column 1, lines 34 - 38; column 3, lines 61 - 64; column 4, lines 54 - 57: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list); and dequeuing the plurality of packet pointers from the multiple physical queues to transmit the plurality of packets onto a second network link (Figure 6; column 4, lines 54 – 57; column 5, lines 20 – 35: data in the memory banks is maintained in the form of queues on a first in first out (FIFO) basis, organized by a link list. The output arbitration subsystem uses the same round-robin weighted process as in the input subsystem to buffer and re-segment the data from a chosen queue memory into an acceptable concatenated form for output).

Regarding claim 16, Rusu discloses all the limitations of claim 15. Additionally, Rusu discloses enqueuing the plurality of packet pointers into the multiple physical queues comprises enqueuing the plurality of packet pointers into the multiple physical queues using a round robin enqueuing scheme between the multiple physical queues (Figure 4, 130 and 131; Figure 5; column 1, lines 34 - 38; column 3, lines 61 - 64;

column 4, lines 54 - 57; column 5, lines 27 - 31: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list the round-robin weighted process is used to provide for storing incoming data, utilizing the link list with the highest priority).

Regarding claim 17, Rusu discloses all the limitations of claim 16. Additionally, Rusu discloses dequeuing the plurality of packet pointers from the multiple physical queues comprises dequeuing the plurality of packet pointers from the multiple physical queues using a round robin dequeuing scheme between the multiple physical queues. (Figure 6; column 4, lines 54 – 57; column 5, lines 20 – 35: data in the memory banks is maintained in the form of queues on a first in first out (FIFO) basis, organized by a link list. The output arbitration subsystem uses the same round-robin weighted process as in the input subsystem to buffer and re-segment the data from a chosen queue memory into an acceptable concatenated form for output).

Regarding claim 18, Rusu discloses all the limitations of claim 15. Additionally, Rusu discloses dequeuing of the plurality of packet pointers from the multiple physical queues is executed in a same order as the enqueuing of the plurality of packet pointers (Figure 6; column 4, lines 54 – 57; column 5, lines 20 – 35: data in the memory banks is maintained in the form of queues on a first in first out (FIFO) basis, organized by a link list. The output arbitration subsystem uses the same round-robin weighted process as

in the input subsystem to buffer and re-segment the data from a chosen queue memory into an acceptable concatenated form for output).

Regarding claim 19, Rusu discloses all the limitations of claim 15. Additionally, Rusu discloses a machine-accessible medium that provides instructions that, if executed by the machine, will cause the machine to perform operations, comprising enqueuing the plurality of packet pointers into the multiple physical queues for each of multiple packet flows, each of the plurality of packet pointers to point to one of the plurality of memory locations temporarily having stored therein one of the plurality of packets received from one of the multiple packet flows (Figures 4, 5, and 7, 130, 131, and 145; column 1, lines 34 - 38; column 3, lines 61 - 64; column 4, lines 54 - 57: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list); and dequeuing the plurality of packet pointers from the multiple physical queues for each of the multiple packet flows to transmit the plurality of packets of each of the multiple packet flows (Figure 6; column 4, lines 54 – 57; column 5, lines 20 – 35: data in the memory banks is maintained in the form of queues on a first in first out (FIFO) basis, organized by a link list. The output arbitration subsystem uses the same round-robin weighted process as in the input subsystem to buffer and re-segment the data from a chosen queue memory into an acceptable concatenated form for output).

Regarding claim 20, Rusu discloses all the limitations of claim 19. Additionally, Rusu discloses the multiple packet flows are all transmitted along multiple network links (Figures 1A, 1B, 1C, 60, 70, 61, and 71).

Regarding claim 21, Rusu discloses all the limitations of claim 15. Additionally, Rusu discloses the multiple physical queues comprise multiple link lists (Figures 4 and 7, 130, 131, and 145).

Regarding claim 23, Rusu discloses a router, comprising a first port to receive a plurality of packets of a packet flow (Figure 1A, 60); a memory unit to temporarily queue the plurality of packets of the packet flow (Figure 1A, 110 and 130: buffer and queue memory bank); a queue manager to enqueue a plurality of packet pointers, each one of the plurality of packet pointers to point to one of the plurality of packets temporarily queued, the queue manager to enqueue the plurality of packet pointers into multiple link lists (Figures 1A, and 2 140; Figure 5; column 1, lines 34 - 38; column 3, lines 61 - 64; column 4, lines 54 - 57: two individual in use link lists, one for each memory or queue bank The queue controller provides for storage of incoming packets a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list); and a second port to transmit the plurality of packets thereon, each of the plurality of packets to be transmitted in response to the queue manager dequeuing one of the plurality of packet pointers (Figure 1A, 71; Figure 6).

Regarding claim 24, Rusu discloses all the limitations of claim 23. Additionally, Rusu discloses the queue manager is further to enqueue the plurality of packet pointers into the multiple link lists using a round robin enqueuing scheme between the multiple link lists (Figure 4, 130 and 131; Figure 5; column 1, lines 34 - 38; column 3, lines 61 - 64; column 4, lines 54 - 57; column 5, lines 27 - 31: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list the round-robin weighted process is used to provide for storing incoming data, utilizing the link list with the highest priority).

Regarding claim 25, Rusu discloses all the limitations of claim 24. Additionally, Rusu discloses the queue manager is further to dequeue the plurality of packet pointers from the multiple link lists in a same order as enqueuing the plurality of packet pointers (Figure 6; column 4, lines 54 - 57; column 5, lines 20 - 35: data in the memory banks is maintained in the form of queues on a first in first out (FIFO) basis, organized by a link list. The output arbitration subsystem uses the same round-robin weighted process as in the input subsystem to buffer and re-segment the data from a chosen queue memory into an acceptable concatenated form for output).

Regarding claim 26, Rusu discloses all the limitations of claim 23. Additionally, Rusu discloses the queue manager comprises hardware entity (column 2, lines 30 - 35: the queue controller is coupled to input subsystems and output processors. The queue controller is also coupled to the queue memory banks).

Regarding claim 27, Rusu discloses all the limitations of claim 26. Additionally, Rusu discloses the queue manager further comprises a software entity (column 2, lines 35 - 41: the queue controller processes stores, and transmits data between input subsystems and output subsystems using the queue memory. The queue controller establishes, maintains, and provides management of the balanced operation dual bank queue operation).

Regarding claim 28, Rusu discloses a system comprising a plurality of optical routers, each of the plurality of optical routers comprising a first port to receive a plurality of packets of a packet flow (Figure 1A, 60); a memory unit to temporarily queue the plurality of packets of the packet flow (Figure 1A, 110 and 130: buffer and queue memory bank); a queue manager to enqueue a plurality of packet pointers, each one of the plurality of packet pointers to point to one of the plurality of packets temporarily queued, the queue manager to enqueue the plurality of packet pointers into multiple physical queues (Figures 1A and 2, 140; column 3, lines 61 - 64; column 4, lines 54 - 57: the queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list); and a second port to transmit the plurality of packets thereon, each of the plurality of packets to be transmitted in response to the queue manager dequeuing one of the plurality of packet pointers (Figure 1A, 71; Figure 6); and a plurality of optical fibers to link the plurality of optical routers into a network, the first port and the second port of each of the plurality of routers each coupled to one of the plurality of optical fibers (column 2, lines 45 – 53).

Regarding claim 29, Rusu discloses all the limitations of claim 28. Additionally, Rusu discloses the queue manager is further to enqueue the plurality of packet pointers into the multiple physical queues using a round robin enqueuing scheme between the multiple physical queues (Figure 4, 130 and 131; Figure 5; column 1, lines 34 - 38; column 3, lines 61 - 64; column 4, lines 54 - 57; column 5, lines 27 - 31: two individual in use link lists, one for each memory or queue bank. The queue controller provides for storage of incoming packets in a specified location in one of the queue memory banks. The queue controller maintains the packets in the first-in-first-out (FIFO) queue that is organized as a link list the round-robin weighted process is used to provide for storing incoming data, utilizing the link list with the highest priority).

Regarding claim 30, Rusu discloses all the limitations of claim 29. Additionally, Rusu discloses the queue manager is further to dequeue the plurality of packet pointers from the multiple physical queues in a same order as enqueuing the plurality of packet pointers (Figure 6; column 4, lines 54 - 57; column 5, lines 20 - 35: data in the memory banks is maintained in the form of queues on a first in first out (FIFO) basis, organized by a link list. The output arbitration subsystem uses the same round-robin weighted process as in the input subsystem to buffer and re-segment the data from a chosen queue memory into an acceptable concatenated form for output).

Allowable Subject Matter

3. Claims 7, 14, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 7, the prior arts do not disclose the relation, PQ = (LQ x N) + Qmult, where PQ represents a link list number of one of the multiple link lists, LQ represents a logical queue number corresponding to one of the multiple packet flows, N represents a number of the multiple link lists per each one of the multiple packet flows, and Qmult differentiates between each one of the multiple link lists of each of the multiple packet flows.

Regarding claim 14, the prior arts do not disclose the relation, PQ = (LQ x N) + Qmult, where PQ represents a physical queue number of one of the corresponding multiple physical queues, LQ represents a logical queue number corresponding to one of the multiple packet inflows, N represents a number of the corresponding multiple physical queues per each of the multiple packet inflows, and Qmult differentiates between each one of the multiple physical queues of each of the multiple packet inflows.

Regarding claim 22, the prior arts do not disclose the relation, PQ = (LQ x N) + Qmult, where PQ represents a link list number of one of the multiple physical queues,

LQ represents a logical queue number corresponding to one of the multiple packet flows, N represents a number of the multiple physical queues per each of the multiple packet flows, and Qmult differentiates between each one of the multiple physical queues of each of the multiple packet flows.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juvena W. Loo whose telephone number is (571) 270-1974. The examiner can normally be reached on Mon.-Thurs : 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frantz Coby can be reached on (571) 272-4017. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juvena W Loo
Examiner
Art Unit 2609

FRANTZ COBY
SUPERVISORY PATENT EXAMINER